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10/549,367	09/14/2005	Nicolaas Lambert	NL03 0267 US1	6175

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
03/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/549,367	LAMBERT ET AL.	
	Examiner	Art Unit	
	DUC T. DOAN	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/21/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-14 have been presented for examination in this application.

Claims 15-20 have been added.

Claims 3 and 14 have been canceled.

Claims 1-2, 4-13 and 15-20 remain pending.

Claims 1-2, 4-13 and 15-20 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Information Disclosure Statement

The Information Disclosure Statements received 1/21/2010 have been considered. See attached PTO-1449(s).

Response to Arguments

Applicant's remarks filed 01/21/2010 have been fully considered but they are mooted in view of mooted in view of new ground(s) of rejection applied with new reference(s) found.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set for in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 01/21/2010 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-5 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al (US 2004/0088513) in view of Deng et al (US Pat. 6795327).

As in claim 1, Biessener discloses a memory device (Fig 7 controller) comprising a memory including a plurality of low-latency, rewritable, non-volatile memory cells (Fig 1 storage system 8, par. 44 memory volatile, non-volatile etc.., the memory has several partitions, par. 52);

a profile storage connected to the memory unit including access information allocated to at least one request profile (Fig 2, partition table par. 56, and information related to a partition such as password etc.. par. 60), said request profile including at least one set of request information elements and said access information indicating whether an access request, which fits a particular request profile, is to be allowed or

rejected (par. 69 partition table 11, i.e. claim's profile storage, comprise partitions tables for users, with specific information for the specific partition / profile such as par. 58 table 1 and password or other information par. 60);

an access control unit connected with said profile storage unit and said memory, (par. 60, controller 6 logic processes request, i.e claim's access control unit, requires connecting for accessing to information in storage and partition table 11); said access control unit configured to ascertain a request profile to an access request using request information of said access request (Fig 5, pars. 69-72, using request's information to clarify the specific section of partition table), said access control unit further configured to determine access rights of said access request in dependence on the access information allocated to the request profile of the access request (pars. 57-58, table 1, partition table information indicates access permission for requests).

Biessener does not expressly disclose the claim's plurality of interfaces in communication with different external memory clients of a universal memory. However, Deng discloses a plurality of interfaces in communication with different external memory clients or communicating according the different memory uses (Fig 1, interface 1-N), wherein the plurality of interfaces are functional units each providing specific access characteristics by allocating a set of request profiles to each interface (Fig 2, 21 and 22 interface units). It would have been obvious to one of ordinary skill in the art at the time of invention to include plurality of interfaces as suggested by Deng in Biessener's system and thereby data can be transferred in several interfaces in an efficiently

manner and thereby further improve overall performance of the system (col. 2 lines 30-55).

As in claim 2, Biessener further discloses wherein said set of request information elements includes at least one set of request information elements (Fig 5, pars. 69-72, a request profile have related information), at least one request information element indicating at least one of: a type of request, an external memory client from which the request originates, a memory section the request is directed to, an access authorization, a password, a request protocol type, a time of request, an interface receiving the request, the length of the request, time span lapsed since a last request, a security class, or a priority class (Fig 2 and 5, partition table par. 56, 69-72, and information related to a partition such as password etc.. par. 60).

As in claim 4, Biessener further discloses wherein at least one of said interfaces is implemented in the form of hardware (Fig 7 and 9, par. 94 discloses storage devices of storage system 8 communicates with controller 6 using interface logic 18. It's further noted that the interface logic 18 represents circuitries to send and receive data over communicating medium 7).

As in claim 5, Biessener further discloses wherein at least one of said interfaces is implemented in the form of software (Fig 7 and 9, par. 94 discloses storage devices of storage system 8 communicates with controller 6 using interface logic 18. It's further noted that the interface logic 18 represents drives logic (i.e software ad hardware), to send and receive data over communicating medium 7).

As in claim 8, Biessener further discloses comprising a supervisor interface adapted to create or change at least one request profile and/or access information allocated thereto, given a predetermined condition (par. 15 an authorized user can have a given/limit access condition to access partitions).

As in claim 9, Biessener further discloses wherein said supervisor interface is adapted to admit or reject external requests for change of a request profile, depending on access information allocated to at least one predetermined change request profile (par. 18, filtering unauthorizing commands requests using configuration information defined by user/administrator).

As in claim 10, Biessener further discloses wherein said profile storage unit comprises a set of access flags, each access flag allocated to a respective request profile, and 20 wherein said access information is given by one of two possible states of an access flag (Table 1, partition states are flags that allow or reject requests for a partition).

As in claim 11, Biessener further discloses wherein said profile storage unit is integrated into said access control unit (par. 55).

As in claim 12, Biessener further discloses wherein said access control unit is adapted to maintain a current copy of said profile storage unit in a predetermined section of said memory (pars. 55-58, table 1, partition table information such as boot partition, is stored in a predetermined section of flash memory such that it can be loaded into the system).

Claims 6-7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al (US 2004/0088513) in view of Deng et al (US Pat. 6795327) and in further view of Kim et al (US Pub. 2001/0015905).

As in claim 6, Biessener and Deng do not expressly disclose the SRAM-type interface. However, Kim discloses an SRAM-type interface adapted to serve separate connections for address data input and user data exchange, respectively, between the memory device and at least one external memory client (par. 23, Fig 2, SRAM interface 150). It would have been obvious to one of ordinary skill in the art at the time of invention to include SRAM interface as suggested by Kim in Biessener's system modified by Deng and thereby memory device is readily adapted to communicated with another commonly and popular interface (par. 23).

As in claim 7, Biessener and Deng do not disclose the claim's aspect of shared connection. However, Kim discloses an I/O-type interface adapted to serve a shared connection for address data input and user data exchange between the memory device and at least one external memory client (par. 23, Fig 2, NAND interface 170). It would have been obvious to one of ordinary skill in the art at the time of invention to include NAND interface as suggested by Kim in Biessener's system modified by Deng and thereby memory device is readily adapted to communicated with another commonly and popular interface (par. 23).

As in claim 13, Biessener and Deng do not expressly disclose the claim's aspect of different ways of memory addressing. However, However, Kim discloses a translation unit adapted to translate between one or more different ways of memory addressing

(par. 23, translation logic translates several addressing of several interfaces). It would have been obvious to one of ordinary skill in the art at the time of invention to include several interfaces as suggested by Kim in Biessener's system modified by Deng and thereby memory device is readily adapted to communicated with several commonly and popular interfaces (par. 23).

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al (US 2004/0088513) in view of Falik et al (US Pat. 7318129).

As in claim 15, Biessener discloses a memory device comprising:

an interface for receiving access requests (par, 81, Fig 7 28 17 18);

a memory cell array having a plurality of low-latency, rewritable, non-volatile memory cells forming at least one memory section (par 44, Fig 7 8 storage system such as memory);

a word-select unit connected between the interface and the memory cell array to provide column selection (inherent column logic of memory array);

a section-select unit connected between the interface and the memory cell array to provide row selection (logic addressing a partition / lines of memory, i.e. claim's row, for partition as disclosed in table 1, par. 58);

a profile storage unit connected to said interface comprising a plurality of request profiles that each represent a profile of an access request (Fig 2, partition tables for users' partitions, pars. 55-56, and information related to a partition such as password etc.. par. 60), wherein each request profile includes:

a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request (par 68, a read or write request from user inherently has read or write information) ;

Biessener does not expressly disclose the claim's flag. However, Falik discloses and an access flag whose state indicates whether a corresponding access request is allowed to access the memory or not allowed to access the memory (c13 line 62 to col. 12, flags for accesses of hosts); an access control unit connected to said profile storage unit and said memory and configured to allow or reject an access request (col. 11 lines 20-40, grant each access paths a set of access levels);

wherein said profile storage unit selects an access flag that corresponds to a request profile in response to an access request that fits the request profile (col. 11 lines 20-40, obtaining flags SMHAP per specific access); and

wherein the access control unit allows or rejects an access request in response to the access flag that is selected by the profile storage unit (col. 11 lines 20-40, allowing or not allowing accessing of specific access is in response to flag SMHAP).

It would have been obvious to one of ordinary skill in the art at the time of invention to include access control and flags as suggested by Falik in Biessener's system and thereby shared memory can be managed efficiently and thereby further improve the overall performance of the system (col. 11 lines 1-22 and abstract).

As in claim 16, Biessener does not expressly disclose the claim's flag. However, Falik discloses wherein the profile storage unit comprises a set of access flags, one

access flag for each row address, such that each access flag governs the access to one row of the memory cell array (col. 13 lines 25-50, SMCORP 404 FCWP registers are access flags for blocks of any size). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Falik in Biessener's system for the same reasons stated above.

As in claim 17, Biessener does not expressly disclose the claim's flag. However, Falik discloses wherein the access flags are fast read-out state registers (col. 13 lines 63 to col. 14 lines 12 SMHAP registers). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Falik in Biessener's system for the same reasons stated above.

As in claim 18, Biessener does not expressly disclose the claim's flag. However, Falik discloses wherein the access control unit operates in a data path to admit or reject a flow of data to or from the memory cell array depending on the state of the corresponding access flag it receives from the profile storage unit (col. 11 lines 20-40, allowing or not allowing accessing of specific access is in response to flag SMHAP). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Falik in Biessener's system for the same reasons stated above.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al (US 2004/0088513) in view of Falik et al (US Pat. 7318129) and in further view of Kim et al (US Pub. 2001/0015905).

As in claim 19, Biessener and Falik do not expressly disclose the claim's several interfaces. However, Deng discloses a plurality of interfaces in communication with

different external memory clients or communicating according the different memory uses (Fig 1, interface 1-N), wherein the plurality of interfaces are functional units each providing specific access characteristics by allocating a set of request profiles to each interface (Fig 2, 21 and 22 interface units). It would have been obvious to one of ordinary skill in the art at the time of invention to include plurality of interfaces as suggested by Deng in Biessener's system modified by Falik and thereby data can be transferred in several interfaces in an efficiently manner and thereby further improve overall performance of the system (col. 2 lines 30-55).

Biessener and Falik and Deng do not expressly disclose the claim's memory mapped interface and an I/O mapped interface. However, Kim discloses memory mapped interface and an I/O mapped interface connected to provide access to the memory cell array (par. 23, Fig 2 memory device adapts to SRAM interface and NAND interface). It would have been obvious to one of ordinary skill in the art at the time of invention to include interfaces as suggested by Kim in Biessener's system modified by Falik and Deng and thereby memory component is readily adapted to communicated with commonly and popular interfaces (par. 23).

As in claim 20, Biessener and Falik and Deng do not expressly disclose the claim's memory mapped interface and an I/O mapped interface. However Kim discloses wherein pins of the memory device are shared by the memory mapped and I/O mapped interfaces (par. 23 Fig 2 pins 130 and 120 are shared for interfaces SRAM 150 and NAND 170. Examiner note: components 140-170 corresponds to claim's memory device).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tuan V. Thai/

Primary Examiner, Art Unit 2185